EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1731	(375/316).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 21:08
S2	76	"PAM-4"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:09
S3	109	PAM near4 ("4" near2 level)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:09
S4	175	S2 or S3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:09
S5	6	S2 WITH slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:15
S6	4	S3 with slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:15
S7	8	S5 or S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:10
S8	8	S2 same slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:42

EAST Search History

S9	4	S3 same slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:15
S10	10	S8 or S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:15
S11	19	S2 and slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:42
S12	19	S3 and slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:42
S13	32	S11 or S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:42
S14	13	S13 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:54
S15	283	"4" near3 level near3 slic$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:01
S16	208	S15 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:02

EAST Search History

S17	0	S16 and PAM	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:55
S18	2	S16 and CMOS	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 21:57
S19	14	S16 and (integrated adj3 circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:04
S20	319	"3" near3 level near3 slic$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:01
S21	242	S20 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:08
S22	2	S21 and PAM	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:03
S23	2	S21 and CMOS	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:03
S24	21	S21 and (integrated adj3 circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:08

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S25	1	CMOS near4 slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:08
S26	13	CMOS with slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:11
S27	4	S26 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:11
S28	40	CMOS same slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:11
S29	1	(US-5517532-$).did.	USPAT	OR	ON	2006/08/29 22:11
S30	24	S28 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:35
S31	1657	center near2 tap near2 resistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:35
S32	12	S31 and slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:35
S33	10	S32 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:40

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S34	1564	S31 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:56
S35	272	S34 and comparat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:56
S36	7	S35 and slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:41
S37	2	S35 and PAM	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:42
S38	122	S35 and differential	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:54
S39	71	S35 and (differential near3 amplifier)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:43
S40	31	S39 and offset	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:44
S41	23	S40 and (CMOS or (integrated near3 circuit))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:44

EAST Search History

S42	43	S31 with comparat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 22:56
S43	37	S42 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:05
S44	484	comparator with slicer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:05
S45	2	S44 and "PAM-4"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:05
S46	11	S44 and PAM	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:05
S47	3	S46 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:10
S48	336	S44 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:36
S49	287	S48 and level	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:10

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S50	0	S49 and (PAM near2 "4")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:11
S51	32	S49 and (level near2 "3")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:11
S52	1	(US-6313885-$).did.	USPAT	OR	ON	2006/08/29 23:25
S53	19	slicer and (first adj2 comparator) and (second adj2 comparator) and (third adj2 comparator)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:38
S54	10	S53 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:49
S55	3	slicer same ((first adj2 comparator) and (second adj2 comparator) and (third adj2 comparator))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:48
S56	69	(integrated adj2 circuit) and (substrate with semiconductor) and (slicer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:49
S57	34	S56 and @pd<"20030708"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 23:49
S58	1	(US-5699386-$).did.	USPAT	OR	ON	2006/08/29 23:58

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1. **A single chip teletext decoder including data slicer**
Lyne, C.R.W.;
Consumer Electronics, 1989. Digest of Technical Papers. ICCE., IEEE 1989 In Conference on
6-9 June 1989 Page(s):164 - 165
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2. **Teletext: a true monochip solution**
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3. **54 MHz switched-capacitor video channel equaliser**
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5. **High performance picture-in-picture (PIP) IC using embedded DRAM tech**
Brett, M.; Wendel, D.;
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6. **High performance picture-in-picture (PIP) IC using embedded DRAM tech**
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22-24 June 1999 Page(s):342 - 343
Digital Object Identifier 10.1109/ICCE.1999.785391
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7. **A mixed-signal 120 MSample/s PRML solution for DVD systems**
Baird, R.; Feyh, G.; Graba, J.; Hood, M.; Keisuke Kato; Kent, M.; Kostelnik, M. Kafai Leung; Yanning Lu; Painter, C.; Patel, K.; Pietruszynski, D.; Romano, P.; Suey Shaw; Supine, L.; Urabe, M.; Sarah Zhu; Zook, C.;
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Digital Object Identifier 10.1109/ISSCC.1999.759084
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8. **QAM/VSB dual mode equalizer design and implementation**
Wu, C.F.; Shiue, M.T.; Huang, C.C.; Jou, S.J.;
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9. **An adaptive analog noise-predictive decision-feedback equalizer**
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Volume 37, Issue 2, Feb. 2002 Page(s):105 - 113
Digital Object Identifier 10.1109/4.982416
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10. **A 2 MHz GFSK IQ receiver for Bluetooth with DC-tolerant bit slicer**
Bang-Sup Song; Cho, T.; Kang, D.; Dow, S.;
Custom Integrated Circuits Conference, 2002. Proceedings of the IEEE 2002
12-15 May 2002 Page(s):431 - 434
Digital Object Identifier 10.1109/CICC.2002.1012865
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11. **A 2.4 GHz Bluetooth transceiver in 0.18 /spl mu/m CMOS**
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12. **Adaptive PRML SOC development for read/write capable optical drives**
Junghyun Lee; Jae-Wook Lee; Jae-Seoung Shim; Hyun-Soo Park;
ASIC/SOC Conference, 2002. 15th Annual IEEE International
25-28 Sept. 2002 Page(s):102 - 106
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13. **Design and implementation of a novel sync processing system for comp signals**
Dengpan Mou; Lares, R.; Wenhao Yan; Rominger, F.; Rothermel, A.;
Consumer Electronics, IEEE Transactions on
Volume 49, Issue 4, Nov. 2003 Page(s):1286 - 1291
Digital Object Identifier 10.1109/TCE.2003.1261231
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14. **High-performance VLSI architecture of adaptive decision feedback equal predictive parallel branch slicer (PPBS) scheme**
Meng-Da Yang; An-Yeu Wu; Jyh-Ting Lai;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 12, Issue 2, Feb. 2004 Page(s):218 - 226
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15. **An improved architecture of the mixed mode clock/data recovery for DVI**
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Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004
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Beukema, T.; Sorna, M.; Selander, K.; Zier, S.; Ji, B.L.; Murfet, P.; Mason, J.; I
Ainspan, H.; Parker, B.; Beakes, M.;
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Digital Object Identifier 10.1109/JSSC.2005.856584
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17. **A 20-Gb/s Adaptive Equalizer in 0.13-$muhbox m$CMOS Technology**
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Solid-State Circuits, IEEE Journal of
Volume 41, Issue 9, Sept. 2006 Page(s):2058 - 2066
Digital Object Identifier 10.1109/JSSC.2006.880629
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